1.    A non-volatile CAM-type memory, comprising:

a multiplicity of memory cells ordered into a matrix of rows and columns;

a word line and a match line associated with every row of cells;

a first and a second bit line associated with every column of cells;

a ground control line and a ground line associated with every row of cells; and

each cell comprising:

a first non-volatile memory element having a control terminal connected to the word line associated with the row containing the cell, a first terminal connected to the first bit line associated with the column containing the cell and a second terminal connected to a match node of the cell, and

a second non-volatile memory element having a control terminal connected to the word line associated with the row containing the cell, a first terminal connected to the second bit line associated with the column containing the cell and a second terminal connected to the match node of the cell;

a first controlled electronic switch connected between the ground line and the match line associated with the row containing the cell and having a control terminal connected to the match node of the cell, and

a second controlled electronic switch connected between the match node of the cell and the ground line associated with the row containing the cell and having a control terminal connected to the ground control line associated with the row containing the cell.

2.    The CAM-type memory of claim 1, wherein the first and the second non-volatile memory element of each cell are transistors of the floating-gate type in which the first terminal is the drain and the second terminal is the source, and the first and the second controlled electronic switch of each cell are MOS transistors.

3.    The CAM-type memory of claim 1, wherein each cell is configured such that:

when the first non-volatile memory element has a low threshold voltage and the second non-volatile memory element has a high threshold voltage, there is memorized a logic 1,

when the first non-volatile memory element has a high threshold voltage and the second non-volatile memory element has a low threshold voltage, there is memorized a logic 0, and

when both the non-volatile memory elements have high threshold voltages, there is memorized a don't care state.

4.    A method of carrying out the search for a binary word stored in a CAM-type memory of the type of claim 1, comprising the following operations:

associating an element of a comparison register with each column of the matrix,

inserting in the comparison register a word to be searched,

comparing the content of the register bit by bit with the content of each row in accordance with the following operations:

applying a first pre-determined voltage to the ground line,

applying a second pre-determined voltage to the match line,

applying a third pre-determined voltage to the word line,

applying to the ground control line a fourth pre-determined voltage sufficient to close the electronic switch and to discharge the match node of the cells of the row and immediately afterwards applying the first pre-determined voltage to the same ground control line,

subsequently biasing the bit lines of every column by applying a pre-determined search voltage to one of the first and the second bit line according to whether the respective bit of the comparison register is in a first or a second logic state,

monitoring the voltage of the match line, and

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generating a match signal whenever the voltage on the match line does not vary or a no-match signal when the voltage on the match line varies.

5.      The method of claim 4, wherein the bit line to which the pre-determined search voltage is not applied during the subsequent operation of biasing the bit lines is left unconnected.

6.      The method of claim 4, wherein a reference voltage is applied to the bit line to which the pre-determined search voltage is not applied during the subsequent operation of biasing the bit lines.

7.      The method of claim 4, wherein

the first pre-determined voltage applied to the ground line amounts to about 0V,

the second pre-determined voltage applied to the match line is in the range of between 0.8V and 1.8V,

the third pre-determined voltage applied to word line amounts to about 4V,

the fourth pre-determined voltage applied to the ground control line is in the range of between 5V and 8V, and

the pre-determined search voltage $V_{SEARCH}$ is in the range of between 1.2V and 2V.

8.      The method of claim 4, wherein

the first pre-determined voltage applied to the ground line amounts to about 1.8V,

the second pre-determined voltage applied to the match line is in the range of between 0V and 0.5V,

the third pre-determined voltage applied to word line amounts to about 4V,

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the fourth pre-determined voltage applied to the ground control line is in the range of between 5V and 8V, and

the pre-determined search voltage $V_{SEARCH}$ is greater than the voltage applied to the ground line.

9.    A memory cell, comprising;

a first transistor having a control gate coupled to a word line, a first terminal coupled to a first bit line, and a second terminal coupled to a first node;

a second transistor having a control gate coupled to the word line, a first terminal coupled to a second bit line, and a second terminal coupled to the first node;

a first switch having a control gate coupled to a control line, a first terminal coupled to the first node, and a second terminal coupled to a voltage source; and

a second switch having a control gate coupled to the first node, a first terminal coupled to the voltage potential, and a second terminal coupled to a match line.

10.    The memory cell of claim 9, wherein the first and second transistors comprise field effect transistors.

11.    The memory cell of claim 9, wherein the first and second switches each comprise a transistor.

12.    The memory cell of claim 9, wherein the first and second transistors and first and second switches are configured such that when the first transistor has a low threshold voltage and the second transistor has a high threshold voltage, there is stored therein a logic 1;

when the first transistor has a high threshold voltage and the second transistor has a low threshold voltage, there is stored therein a logic 0; and

when the first and second transistors each have high threshold voltages, there is stored therein a don't care state.

13. A memory, comprising:

a plurality of memory cells arranged in rows and columns to form a memory matrix, each memory cell comprising:

a first transistor having a control gate coupled to a word line, a first terminal coupled to a first bit line, and a second terminal coupled to a first node;

a second transistor having a control gate coupled to the word line, a first terminal coupled to a second bit line, and a second terminal coupled to the first node;

a third transistor having a control gate coupled to a control line, a first terminal coupled to the first node, and a second terminal coupled to a voltage source; and

a fourth transistor having a control gate coupled to the first node, a first terminal coupled to the voltage potential, and a second terminal coupled to a match line.

14. The memory of claim 13, wherein the first and second transistors comprise field effect transistors.

15. The memory of claim 13, wherein each memory cell is configured such that when the first transistor has a low threshold voltage and the second transistor has a high threshold voltage, there is stored therein a logic 1;

when the first transistor has a high threshold voltage and the second transistor has a low threshold voltage, there is stored therein a logic 0; and

when the first and second transistors each have high threshold voltages, there is stored therein a don't care state.

16.    A computer system, comprising:

a microprocessor and a memory associated therewith, the memory comprising a plurality of cells arranged in rows and columns to form a matrix, each cell comprising:

a first transistor having a control gate coupled to a word line, a first terminal coupled to a first bit line, and a second terminal coupled to a first node;

a second transistor having a control gate coupled to the word line, a first terminal coupled to a second bit line, and a second terminal coupled to the first node;

a third transistor having a control gate coupled to a control line, a first terminal coupled to the first node, and a second terminal coupled to a voltage source; and

a fourth transistor having a control gate coupled to the first node, a first terminal coupled to the voltage potential, and a second terminal coupled to a match line.


17.    The computer system of claim 16, wherein the first and second transistors comprise field effect transistors.


18.    The computer system of claim 16, wherein each memory cell is configured such that when the first transistor has a low threshold voltage and the second transistor has a high threshold voltage, there is stored therein a logic 1;

when the first transistor has a high threshold voltage and the second transistor has a low threshold voltage, there is stored therein a logic 0; and

when the first and second transistors each have high threshold voltages, there is stored therein a don't care state.


19.    A method of searching a memory, the memory having a plurality of memory cells arranged in rows and columns, each cell having a first transistor having a

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control gate coupled to a word line, a first terminal coupled to a first bit line, and a second terminal coupled to a first node;

a second transistor having a control gate coupled to the word line, a first terminal coupled to a second bit line, and a second terminal coupled to the first node;

a first switch having a control gate coupled to a control line, a first terminal coupled to the first node, and a second terminal coupled to a voltage source; and

a second switch having a control gate coupled to the first node, a first terminal coupled to the voltage potential, and a second terminal coupled to a match line, the method comprising:

comparing the contents of a comparison register associated with each column of the memory matrix bit by bit with the content of each row of the memory matrix in accordance with the following operations:

applying a first pre-determined voltage to the voltage potential;

applying a second pre-determined voltage to the match line;

applying a third pre-determined voltage to the word line;

applying to the control line a fourth pre-determined voltage sufficient to close the second electronic switch and to discharge the first node of the cells of the row and immediately afterwards applying the first pre-determined voltage to the same control line;

subsequently biasing the first and second bit lines of every column by applying a pre-determined search voltage to one of the first and the second bit lines according to whether the respective bit of the comparison register is in a first or a second logic state;

monitoring the voltage on the match line; and

generating a match signal whenever the voltage on the match line does not vary and generating a no-match signal whenever the voltage on the match line varies.